Pulse Regeneration in the Gigabit-per-Second Range Using a Diode Differential Regenerator

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Abstract—**A clocked pulse regenerator circuit (diode differential regenerator (DDR)) is described which employs a modified hybrid tee, step recovery diodes, and bipolar transistors. For the first time a hybrid tee is used in ultra broad-band digital applications. Signal pulses with bit rates up into the gigabit-per-second range are regenerated, the shape of the input pulses having no direct influence on the shape of the output pulses. Only the charge of the input signals determines the amplitudes of the output pulses. At a signal bit rate of 1 Gbit/s an insertion voltage gain of 20 dB was obtained. Operating the DDR in a push–pull mode the voltage gain is doubled to 26 dB. Because the output pulses of the DDR are very narrow the circuit can be used in time-division multiplexers providing output pulse streams with bit rates up to 16 Gbit/s and amplitudes of several volts across a load of 50 Ω. The internal behavior of the DDR is analyzed, among other things by the results of computer simulations. Calculations for optimizing the employed components are given.**

I. Introduction

FOR COMMUNICATION systems a continuous trend to digital techniques can be observed. Furthermore, the interest in highest transmitted bit rates has considerably increased. In this paper a pulse regenerator circuit for possible applications in digital (optical) PCM-type communication systems with bit rates in the gigabit-per-second range is described. The considered circuit employs an ultra broad-band modified hybrid tee [1], step recovery diodes, and bipolar transistors.

In high-rate PCM communication systems the signal pulses are attenuated and broadened on the way by the transmission lines. Therefore, such systems must include pulse regenerators, which effect an amplification and both a reshaping and retiming of their input pulses.

In this paper, such a (clocked) regenerator circuit is described providing an amplification of 20 dB at a bit rate of the signal pulses of 1 Gbit/s. The behavior of the circuit is described both as a function of the supply voltages and the important parameters of the employed components. Computer simulations were used for both the description of the internal behavior of the pulse regenerator circuit and the estimation of the optimum component parameters.

The reshaping of the input pulses implies their essential shortening, therefore, these regenerators can be well employed in time-division multiplexers. Such multiplexers are essential circuits in PCM communication systems. They combine several data streams of a low bit rate to a higher bit-rate output bit stream. The multiplexers developed here produce both return to zero (RZ)-format output signals up to 7.84 Gbit/s [18], [19] and nonreturn to zero (NRZ)-format output signals up to 16 Gbit/s [20]. The output voltages amount to several volts.

Manuscript received April 16, 1979; revised October 2, 1979. This work was supported by the Deutsche Forschungsgemeinschaft (DFG).

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II. Principle of Operation

The described pulse regenerator is a clocked circuit containing an extremely broad-band hybrid tee [1], [2] (see Fig. 1). A hybrid junction can be defined as a "waveguide arrangement (including coaxial transmission lines) with four branches which, when the branches are properly terminated, has the property that energy can be transferred from any one branch into only two of the remaining three" [3]. A hybrid tee is reflectionless for a wave propagating into the junction from any branch when the other three branches are matched terminated [3].

A hybrid tee can be described by its scattering matrix as follows (see Fig. 1):

$$\begin{bmatrix} b_3 \\ b_4 \\ b_a \\ b_b \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_3 \\ a_4 \\ a_a \\ a_b \end{bmatrix}. \tag{1}$$

The bandwidths of at most about 3 octaves of well-known hybrid tees are relatively small, therefore, these elements have not yet been used in digital applications like, e.g., in broad-band PCM communication systems. The here employed hybrid tee [1], [2], however, is well suited for such applications by virtue of its very high bandwidth of more than 3 decades. By a modification of this hybrid tee its bandwidth was increased to more than 5 decades [1].

The principle circuitry to employ the hybrid tee in pulse regenerators is shown in Fig. 2. The energy for such a regenerator stage is supplied by a sinusoidal pump (clock), connected to line a. The output line b is terminated with the load 1 and the lines 3 and 4 with their reflection coefficients ρ_3 and ρ_4, respectively. The transmission behavior of the resulting two-port is given by

$$\begin{bmatrix} b_a \\ b_b \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \rho_3 - \rho_4 & \rho_3 + \rho_4 \\ \rho_3 + \rho_4 & \rho_3 - \rho_4 \end{bmatrix} \begin{bmatrix} a_a \\ a_b \end{bmatrix}. \tag{2}$$

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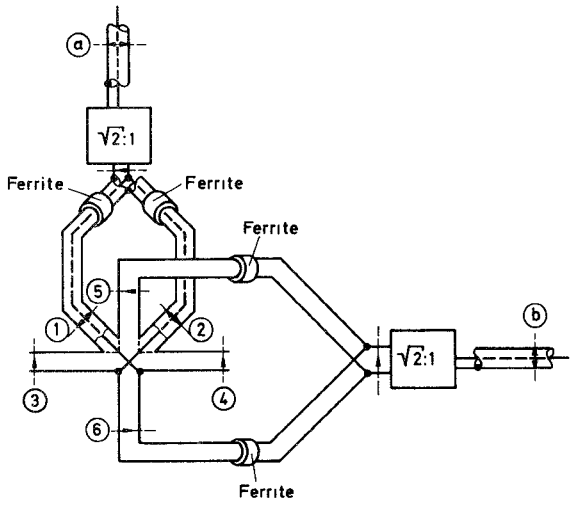

Fig. 1. Circuit of the hybrid tee.

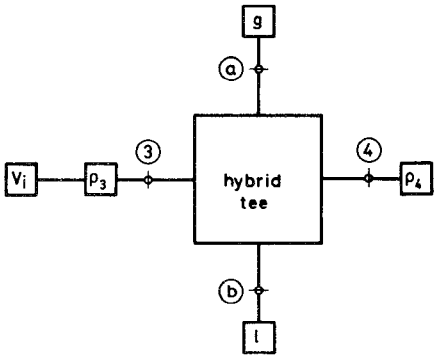

Fig. 2. Principle circuitry of the hybrid tee applicated in a pulse regenerator.

Because the hybrid tee is operated only in one direction with the input line a and the output line b, the transmission behavior of this circuit is determined—with matched termination of the output line b—by the equation

$$b_b = \frac{1}{2}(\rho_3 - \rho_4)a_a. \tag{3}$$

The modified hybrid tee is shown in Fig. 3. It consists of a lumped branching point [4], [5]—constituting a bridge circuit—and either a transformer or a power divider. The lower cutoff frequency can easily be shifted to below 55 kHz. The upper cutoff frequency amounts to 7 GHz and, between the line 3 or 4 and lines 5 or 6, to approximately 12 GHz.

In the modified version of the hybrid tee—the output transformer in line 6 is avoided [1]—the circuits generating the reflection coefficients ρ_3 and ρ_4 can be positioned close to the branching point (at a distance of $1 \cdots 2$ mm). In this case no essential delay times exist between them. Therefore, the operation of this circuit can be calculated by a quasi-stationary approach. That is, the currents in the lines 3, 4, 5, and 6 are calculated as a function of the voltage $V_a/2$ applied to line a, yielding—with matched

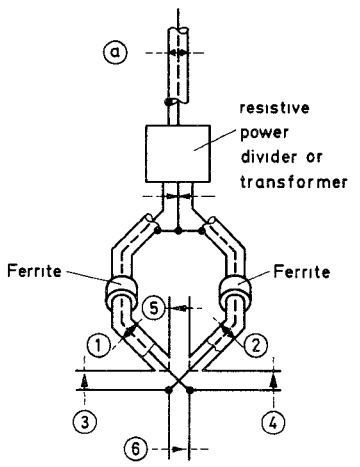

Fig. 3. Modified circuit of the hybrid tee.

output lines 5 and 6—

$$i_3 = \frac{1}{Z_1 + Z_3}\frac{V_a}{\sqrt{2}} \tag{4}$$

$$i_4 = \frac{1}{Z_1 + Z_4}\frac{V_a}{\sqrt{2}} \tag{5}$$

$$i_5 = i_6 = \frac{1}{2}\frac{Z_3 - Z_4}{(Z_1 + Z_3)(Z_1 + Z_4)}\frac{V_a}{\sqrt{2}}. \tag{6}$$

Z_3 is the load of line 3 and Z_4 that of line 4. Z_1 is the characteristic impedance of line 1 being equal to that of line 2 ($Z_1 = Z_2$).

The reflection coefficients and the reflective loads in lines 3 and 4, realized by one step recovery diode (SRD) each, are current controlled: ρ_4 only by the pump current and ρ_3 by both the pump current and the current of an applied signal V_i. Whenever no input signal V_i occurs, ρ_3 is equal to ρ_4, and the output voltage across the load (V_1) is zero. An input signal distorts the symmetry of the circuit; the reflection coefficients are unequal for a short time during which the pump voltage is transferred to the output line b ($V_1 \neq 0$), see Fig. 2.

For realizing the reflection coefficients, SRD's are well suited because:

1) the dynamic impedance of a reverse biased diode is even in the subnanosecond range very much higher than that of a conducting diode,
2) the transient time can be very short (about 50 ps),
3) the transients of the diodes can be shifted in time by choosing appropriate diode currents.

Fig. 4(a) shows the pulse regenerator circuit employing the modified hybrid tee and two (identical) SRD's (Aertech, A4S 008, $C_{j0} = 0.7$ pF (junction capacitance at 0 V), $\tau \simeq 15$ ns (carrier lifetime)). The pump voltage, feeding line a, is divided into halves and then transferred exclusively into the lines 3 and 4. A transformer (line transformer) connects line a with the lines 1 and 2, but is not shown in Fig. 4(a) for clarity. Under the condition of continuously reverse-biased diodes—caused by the voltages V_1 and V_2—the sinusoidal pump voltages V_{p3} and

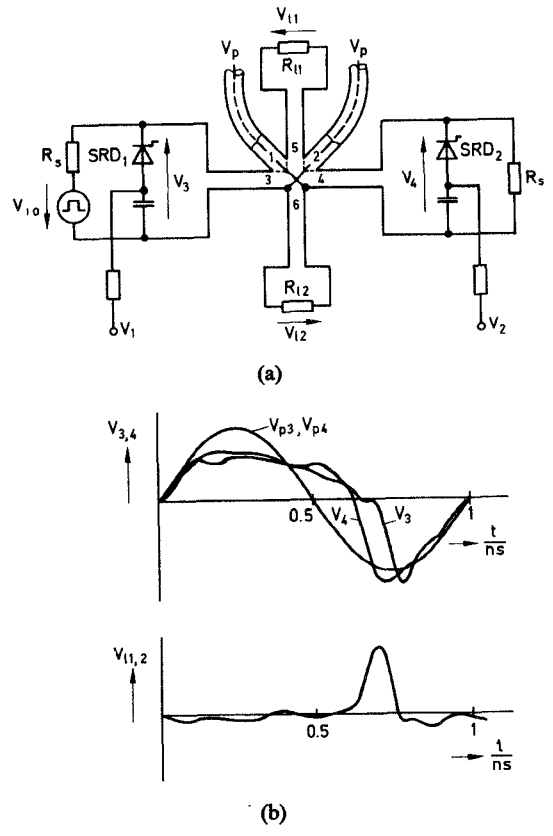

Fig. 4. (a) Circuit of the pulse regenerator employing the modified hybrid tee. (b) Voltages of the pulse regenerator measured at a bit rate of the input signals of 1 Gbit/s.

V_{p4} appear undistorted on the lines 3 and 4. These (measured) voltages are shown in Fig. 4(b). There they have a frequency of 1 GHz. If the SRD's are suitably biased—by V_1 and V_2—both diodes are identically charged by a positive pump half-wave and discharged by a negative one. In this case their impedances are equal to one another at any time. Therefore, the output voltages on the lines 5 and 6 are always zero.

If an input signal V_{i0} occurs within the conducting time of diode SRD_1 the pulse charge is stored in its diffusion capacitance. With a negative input pulse ($V_{i0}<0$) the total charge of SRD_1 is enlarged compared to that of SRD_2. Thus SRD_1 changes to the cutoff state a short time later than SRD_2. Under these conditions the voltages V_3 and V_4 on the lines 3 and 4, respectively, have the shapes shown in Fig. 4(b). Only during the short time of unequal diode impedances output signals (V_{11} and V_{12}) are generated.

Output signals can be generated in three ways.

1) The bias voltages are unequal to one another and no input signals are applied. In this case the circuit is operated as pulse generator [6]. The output signals can have any pulse repetition frequency up to about 5 GHz, determined only by the pump frequency. The amplitude, half-width, and polarity of the output pulses are adjusted by the bias voltages V_1 and V_2.

2) The voltages V_1 and V_2 are equal and input signals occur.

3) The voltages V_1 and V_2 are unequal in such a way that an applied signal pulse makes the SRD's change to the cutoff state simultaneously and suppresses the generation of the two output pulses. The output pulses occur only when no input signal has appeared.

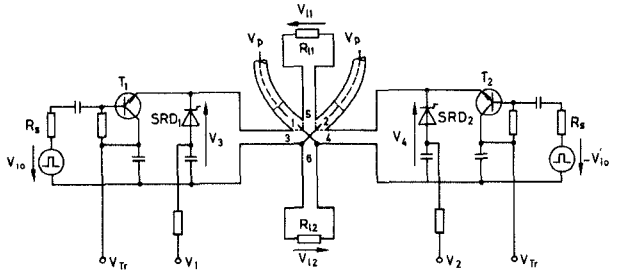

Fig. 5. Extended pulse-regenerator circuit (diode differential regenerator (DDR)).

In cases 2) and 3) the circuit is used as pulse regenerator. It can also be operated in a push–pull mode by connecting a second input signal source ($-V_{i0}$) to line 4 (see Fig. 4(a)). In this case the step recovery diode SRD_1 is, e.g., additionally charged by a negative input signal ($V_{i0}<0$) and SRD_2 is discharged by $-V_{i0}>0$. So the charge difference of both SRD's is doubled and thereby the charge of the output pulses. If the widths of the output pulses are held at a constant value, their amplitudes are doubled.

In the circuit of Fig. 4(a) the SRD's are directly connected to the input signal source(s). Because of the low dynamic impedances of the conducting diodes (series inductances of about 1 nH, bulk resistances of 1 Ω, and very large diffusion capacitances) the signal sources are mismatched. For matching diodes and signal sources, transformers must be inserted. In the final pulse regenerator circuit, fast switching bipolar transistors are used (NEC, V 981 S, $f_T=8$ GHz), operated as emitter followers (Fig. 5).

The resulting circuit can be divided into two parts: at first current gain or charge gain, respectively, is effected by the transistors and then, voltage gain along with a reshaping and retiming of the signal pulses is obtained in the SRD's in conjunction with the modified hybrid tee. Together this results in an essential power gain. The extended circuit is termed "diode differential regenerator, (DDR)."

Presuming that input and output pulses have identical shapes (no push–pull operation) and that the whole input signal charges are stored in the SRD's, the insertion charge, voltage, and power gains (v_q, v_u, and v_p, respectively) can be stated as follows [7]:

$$v_q = 2\frac{V_1}{V_i}\frac{T_{p1}}{T_{pi}} \tag{7}$$

$$v_u = \frac{1}{2} v_q \frac{T_{pi}}{T_{p1}} \tag{8}$$

$$v_p = \frac{1}{2} v_q^2 \frac{T_{pi}}{T_{p1}}. \tag{9}$$

V_i is the amplitude of the input signals measured across a reference load of 50 Ω. T_{pi} is the half-width of the input pulses and T_{p1} that of the output pulses. As can be seen both v_u and v_p—e.g., at a given v_q and T_{pi} in a particular communication system—are inversely proportional to T_{p1}.

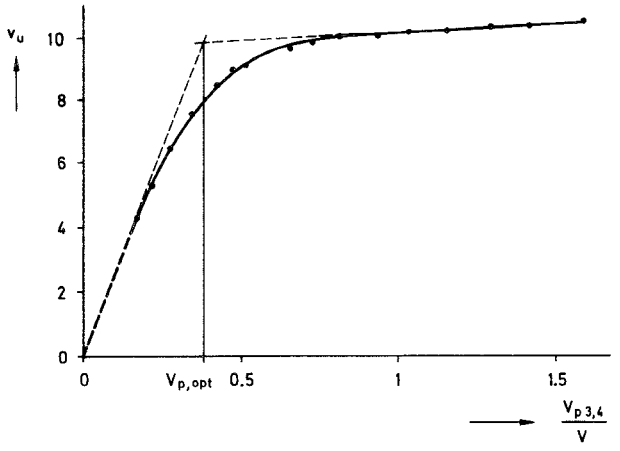

Fig. 6. Insertion voltage gain (v_u) of the DDR versus the amplitudes of the applied (undistorted) pump voltages ($V_{p3,4}$) measured in lines 3 and 4, respectively (bit rate: 1 Gbit/s).

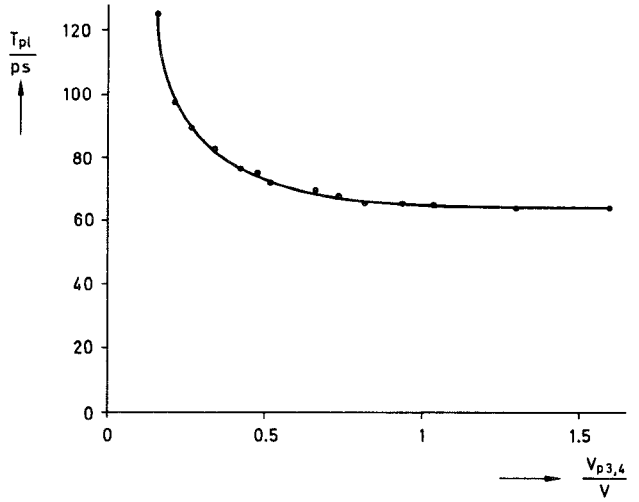

Fig. 7. Output-pulse half-widths (T_{p1}) versus the amplitudes of the undistorted pump voltages $V_{p3,4}$ in lines 3 and 4 (bit rate: 1 Gbit/s).

Because both SRD's are working in a shunt mode, very short rise times (t_r) of the diode voltages can be reached ($t_r \simeq 50$ ps). This leads to very short output-pulse half-widths of less than 100 ps (see Fig. 4(b)). The minimum output-pulse half-width was measured to $T_{p1} = 63$ ps (bit rate: 1 Gbit/s).

With given input signal shapes—e.g., in a communication system—the half-width of the output pulses of the DDR, and consequently the gain, are functions of the applied pump-voltage amplitude. Fig. 6 presents the (measured) typical behavior of voltage gain versus amplitude of the (undistorted) pump voltages ($V_{p3,4}$) obtained in lines 3 and 4. Fig. 7 shows the output-pulse half-widths, again versus $V_{p3,4}$. For obtaining these curves the DDR was operated with one signal source (no push–pull mode) ($V_i = V_{i0}/2 = 18$ mV, $T_{pi} = 475$ ps).

At low pump voltages the output pulses are broad and of low amplitudes. With increasing pump voltages the output pulses become shorter—because the signal charge is recalled faster—and their amplitudes are increased. The charge gain (refer to (7)) is nearly constant ($v_q = 2.66$). The minimum half-width of the output pulses is determined by the rise times of the SRD's and by the upper cutoff frequency of the modified hybrid tee. Both factors limit the maximum insertion voltage gain to about 10 (20 dB).

An optimum operating point ($V_{P,opt}$) can be defined [7] (see Figs. 6 and 7). It is characterized by the fact that the end of the switching process of one diode coincides with the beginning of the switching process of the other diode. In this case the signal-to-noise ratio of the DDR reaches a maximum.

Experimental results [8]–[11] show an essential pulse amplification ($v_u = 20$ dB) in conjunction with a reshaping and retiming of the input signals at a bit rate of 1 Gbit/s. One possible application of the DDR is given in optical PCM communication systems with a bit rate in the gigabit-per-second range [11], where DH-laser diodes, optical fibers, and avalanche-photo diodes (detectors) are used.

III. Description of the Diode Differential Regenerator (DDR)

In the past some basic properties of the DDR were published [7]–[11] (also layout details [1], [7], [8]), therefore, they may be quoted only briefly in this paper.

1) The DDR is charge controlled.

2) Input and output signals are decoupled in time. At a bit rate of 1.12 Gbit/s the conducting times of the SRD's were about 650 ps.

3) The retiming of the output pulses is determined by the timing of the pump voltage relative to the input signals. This temporal relationship has to be ensured, e.g., by a phase-locked loop (PLL).

4) An optimum operation point can be defined at which one SRD begins its switching process when the other diode has just ended it.

5) Employing a transformer in the pump-input line a, the applied pump voltage (V_a) in the optimum operation point of the DDR is about $V_a \simeq \sqrt{2}\ V_1$.

6) The minimum input-signal amplitude is as low as a few millivolts. It is limited by the minimum permissible signal-to-noise ratio of the output signals.

7) The maximum output-pulse amplitude is about 1 V and is given by the maximum permissible power dissipation of the employed transistors (NEC, V 981 S).

In this section the typical internal behavior of the DDR is described using measured curves as well as computed diagrams of a numerical simulation with the program REGENT [12]. Fig. 8 shows measured input and output signals of the DDR. There the circuit was operated only with one input signal source ($-V_{i0}$) delivering input pulses ($V_i = 22.5$ mV—measured at a reference load of 50 Ω; $T_{pi} = 580$ ps) with a bit rate of 1.12 Gb/s. The regenerated output signals ($V_1 = 235$ mV, $T_{p1} = 73$ ps) are shown in the lower trace of Fig. 8. The insertion voltage gain reaches the value of $v_u = 10.44$ (20.5 dB) and the insertion charge gain is $v_q = 2.6$ (regarding both output pulses). With these values the insertion power gain is $v_p = 22.6$ (13.6 dB). In push–pull operation the insertion voltage gain can be doubled to 26.5 dB.

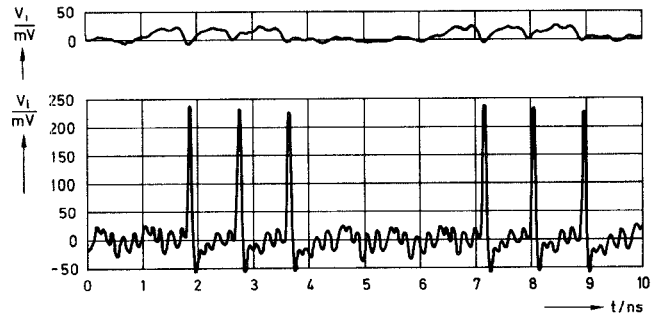

Fig. 8. Measured input pulses (V_i) and output pulses (V_1) of the diode differential regenerator at a bit rate of 1.12 Gbit/s.

For the numerical simulation the employed SRD's and transistors are described by their equivalent circuits which are shown in Fig. 9. The diodes are encapsulated in mini-LID cases, with (series) bond inductivities of $L \simeq 1$ nH. The charges stored in the diodes are calculated by

$$Q = C_{D0} m_c V_T \left(\exp \frac{V_d}{m_c V_T} - 1 \right) + C_{sp0} \frac{V_D}{\gamma - 1} \left[\left(1 - \frac{V_d}{V_D} \right)^{1-\gamma} - 1 \right]. \quad (10)$$

The first term of (10) describes the charge stored in the diffusion capacitance and the second term that in the junction capacitance of an SRD. For the used diodes (Aertech, A4S 008), the parameters are V_d: diode voltage, $C_{D0} = 9.25 \times 10^{-8}$ pF (diffusion capacitance at $V_d = 0$ V), $m_c = 1.35$, $V_T = 25.9$ mV (thermal voltage), $C_{sp0} = 0.77$ pF (junction capacitance at $V_d = 0$ V), V_D: assumed to 1 V (diffusion voltage), and $\gamma = 0.52$. The employed fast switching bipolar transistors have a current gain–bandwidth product of $f_T = 8$ GHz and a short-circuit current gain for low frequencies of $B_0 = 71$.

In Fig. 10 computed voltages and currents of the DDR are presented. Fig. 10(a) shows the input signal, approximated to the measured input pulses presented in Fig. 8. The output pulses (Fig. 10(d)) are a little shorter ($T_{p1} = 65$ ps) and with an amplitude of $V_1 = 300$ mV higher than the measured ones. These (relatively small) differences are caused by the use of the simplified equivalent circuits of the SRD's. The simulated diodes switch somewhat faster into the cutoff state than real SRD's, because effects such as "ramping" and "rounding" [13]–[17] cannot be described by the employed equivalent circuits.

Fig. 10(b) presents computed voltages V_3 and V_4 in lines 3 and 4, respectively. The undisturbed pump voltages V_{p3} and V_{p4} are shown for $t < 1.8$ ns. With properly biased diodes (by V_1 and V_2) the voltages V_3 and V_4 are generated. As in the experiment (Fig. 8), the diodes are discharged when the pump voltages reach their maxima. The diode cutoff voltages are built up by resonant half-waves which are caused by the series inductances and junction capacitances of the diodes. At the end of the first half-wave the diodes change into the conducting state and the oscillations vanish. The amplitudes of these resonant half-waves amount to about twice the corresponding pump voltages because the resonant loops are weakly

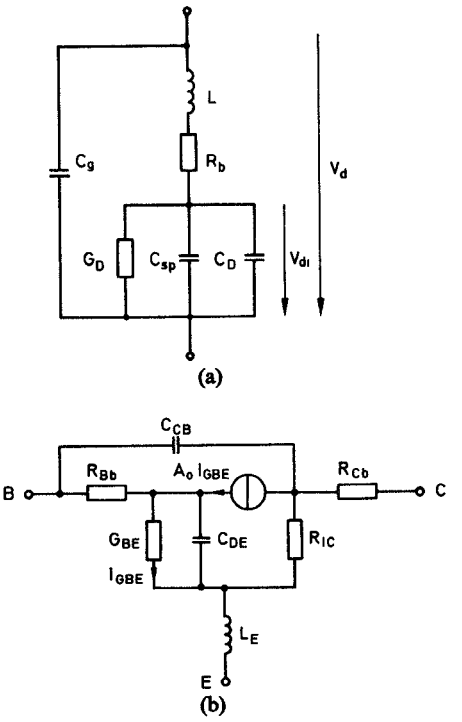

Fig. 9. Equivalent circuit of the step recovery diode (a) and the transistor (b).

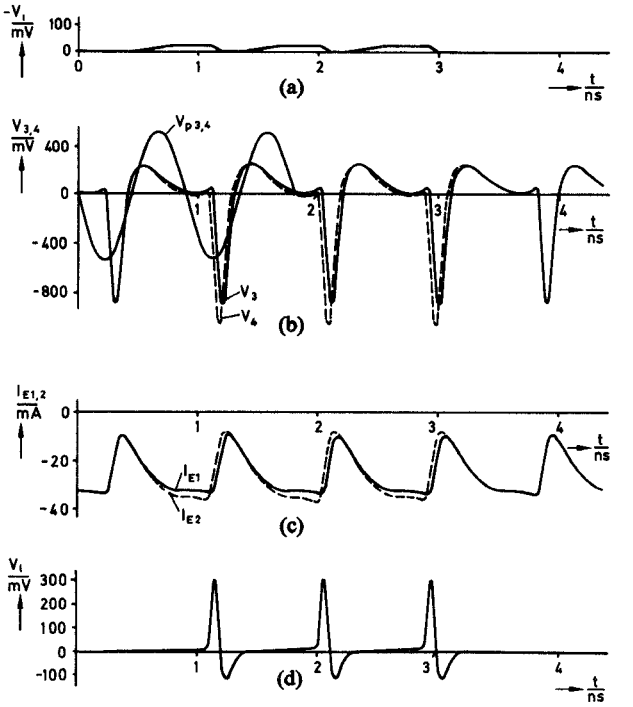

Fig. 10. Computed voltages and currents of the DDR. (a) Input signals. (b) Voltages in the lines 3 and 4. (c) Currents at the emitters of the transistors. (d) Output signals.

damped. This is due to the transforming down of both the internal resistance of the input signal source and the reference resistance (R_s) by the emitter followers.

The widths of the resonant half-waves, as obtained by the simulation, are about 100 ps. Measured widths—at the bases of the transistors—amounted to 130 ps. Each of

these times are constant and, therefore, independent of the switching points of the diodes. However, if the series inductances of the diodes are made smaller in the simulation, the half-widths decrease, too. In the limiting case of vanishing inductance values the oscillations also vanish, and the diode voltages approximate the sinusoidal pump voltages while the diodes are cut off.

The output voltages are generated by the voltage difference $V_3 - V_4$ which is caused by the difference of the reflection coefficients $\rho_3 - \rho_4$ (see (3)). During the trailing edges of the resonant half-waves the difference $V_3 - V_4$ is reversed. This leads to unwanted pulses of opposite polarity lagging the output signals (see Fig. 10(d) and Fig. 8). In the measured curve the lagging pulses have an amplitude of about 25 percent of the signal pulse amplitudes, less than in the computer simulation. This, too, is caused by the simplified equivalent circuits used for simulation leading the SRD's to more undamped resonant oscillations.

The charge gain of the DDR can be calculated by means of Fig. 11. In this figure the essential (computed) pulse charges of an input signal are shown (refer to Fig. 10). The total charge of an input signal flowing through a reference resistor of 50 Ω is $Q_i = 0.257$ pC. The base of the transistor (T_2), however, receives only the charge $Q_B = 0.08$ pC (curve 1), measured in the time of conducting diode SRD_2 ($t < 1.1$ ns). The signal current delivered by the emitter of the transistor T_2 in the same time carries the signal charge of $Q_E = 1.12$ pC (curve 2). Therefore, the transistor shows a charge gain (average gain) of $v_{qTr} = 14$. The signal charge flowing into SRD_2 equals the stored charge in the diffusion capacitance and amounts to $Q_{SRD} = 0.9$ pC (curve 3). Losses caused by recombination in the diode are less than 1 percent of the stored charge and are, therefore, negligible (carrier lifetime of the employed SRD's: $\tau = 15$ ns). The difference $Q_{SRD} - Q_E = 0.22$ pC reaches the branching point of the modified hybrid tee and is not stored.

In the time interval from 1.1 ns to 1.2 ns the output pulses are generated, subsequently the lagging pulses (1.2 ns $\cdots$ 1.4 ns). At first the stored signal charge is removed. In the following the difference charge of the SRD's is changed to $Q_{SRD} = -0.38$ pC. This negative difference of charge is stored in the junction capacitances of the SRD's and causes the (negative) lagging pulses.

During the time the output pulses occur (1.1 ns $\cdots$ 1.2 ns), the combined signal charge of both output pulses amounts to $Q_1 = 0.77$ pC (curve 4). The total signal charge is reduced by the lagging pulses.

As can be seen from curve 2, a nonnegligible part of the stored signal charge flows back into the emitters of the transistors ($Q_{Er} = 0.72$ pC), and is thus lost. This charge loss occurs in the time interval from 1.13 ns to 1.3 ns. The reasons for this can be explained by the following considerations. The currents of the output pulses (1.1 ns $\cdots$ 1.2 ns) contain two components (i_3 and i_4). Combining (4), (5), and (6) yields

$$i_5 = i_6 = 0.5(i_4 - i_3). \tag{11}$$

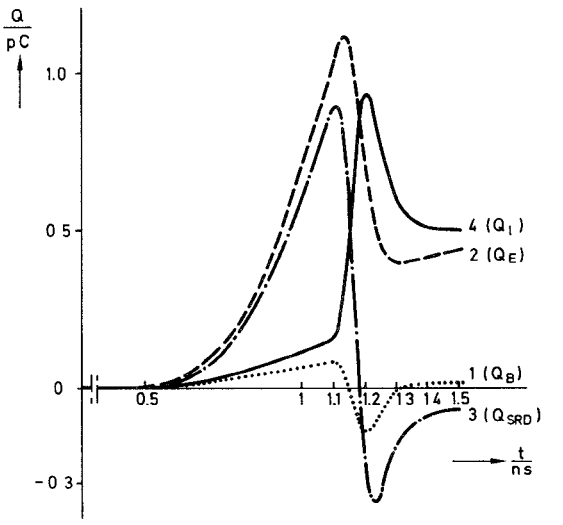

Fig. 11. Computed signal charges of the DDR in the operation mode represented in Fig. 10.

Caused by the input signal $-V_{i0} > 0$, SRD_2 goes into the cutoff state a short time before SRD_1. In the time of different diode impedances the current i_3 is, therefore, determined by the dynamic impedance of the conducting diode SRD_1, shunted by the transformed resistance of the reference resistor (R_s) in line 3 (see (4)). I_4 is determined only by the transformed internal resistance of the signal source (R_s) in line 4 (see (5)). A part of the current i_3 (i_{SRD1}) carries the signal charge. In the output lines 5 and 6 the total charge of i_3 is reduced by the current i_4 which flows through the impedance Z_4 in line 4 (see Fig. 12). The charge gain obtained for the time when output pulses are generated, can be written as

$$v_{qd} = \frac{\int_{t_1}^{t_2} (i_5 + i_6)\, dt}{\int_{t_1}^{t_2} (-i_3)\, dt} \tag{12}$$

where t_1 denotes the start and t_2 the end of the output pulses. Assuming that i_5, i_6, and $i_4 - i_3$ are of equal shape in the interesting interval, (12) reduces to

$$v_{qd} = \frac{I_4 - I_3}{-I_3} \tag{13}$$

where I_3 and I_4 denote the amplitudes of the currents i_3 and i_4, respectively.

Fig. 12 shows the equivalent circuit of the DDR resulting from (4) and (5). The transistors are represented by transformers with a transformation ratio of $\ddot{u}$. With $V_{pa} = \sqrt{2}\, V_{p3} = \sqrt{2}\, V_{p4}$ and the dynamic impedance $Z_3 \simeq Z_{SRD1} \simeq 0$, Fig. 12 yields

$$i_3 = \frac{1}{Z_1}(2V_{p3} - V_3)$$

$$i_4 = \frac{1}{Z_1 + R_s/\ddot{u}^2} 2V_{p4}. \tag{14}$$

The current i_{SRD1}—flowing through SRD_1—carries the signal charge, i_{SRD1} being smaller than i_3 which de-

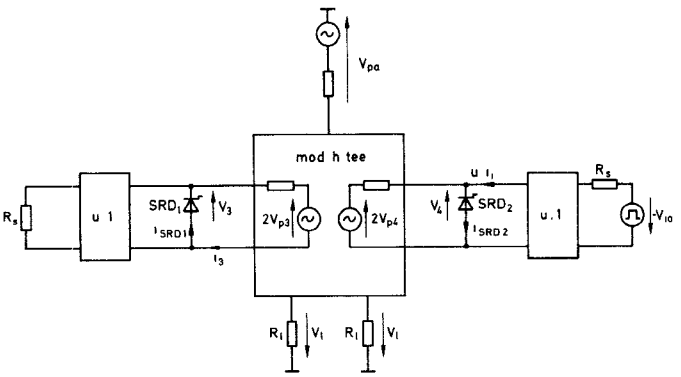

Fig. 12. Equivalent circuit of the DDR for calculating the essential contributions to the charge gain.

termines—together with i_4—the output signal charge:

$$i_{\mathrm{SRD1}} = \frac{1}{Z_1}(2V_{p3} - V_3) - V_3\frac{\ddot{u}^2}{R_s}. \tag{15}$$

Inserting (14) into (13) yields with $V_{p3} = V_{p4} = V_p$, $R_s = Z_1$, and $\ddot{u} \to \overline{\ddot{u}_{\mathrm{Tr}}}$ (average value of the transformation ratio in the time interval of t_1 to t_2)

$$v_{qd} = 1 - \frac{1}{\left(1 + 1/\overline{\ddot{u}_{\mathrm{Tr}}}^2\right)(1 - 0.5V_3/V_p)}. \tag{16}$$

V_3 is the voltage on line 3—containing the conducting SRD_1—in the time of different diode impedances.

With these considerations there are three charge loss mechanisms in the DDR:

1) During the charging phase of the SRD's a part of the signal charge ($\simeq$20 percent), delivered by the transistor is not stored because Z_{SRD} of the conducting diode is not zero.

2) During the time when the output pulses are generated, loss is caused by the charge flowing back into the transformer of that line which carries the switched-off SRD. With $R_s = Z_1$ and $\ddot{u} > 1$ this loss in general amounts to more than 50 percent of the stored signal charge.

3) Loss by the lagging pulses. (As can be seen from Fig. 8 this loss can be held small).

The main losses are those of point 2), being a function of the transformation ratio $\ddot{u}$ of the transformers. Therefore, optimizing criterions for the transformers will be given.

During the charging time of the input signals ($-V_{i0}$) (see Fig. 12), $\overline{i_{\mathrm{SRD2}}} = \overline{\ddot{u}_{\mathrm{Tr}} i_i}$ leads to a charge gain of the transformers of

$$v_{q\mathrm{Tr}} = \frac{\overline{i_{\mathrm{SRD2}}}}{\overline{i_i}} = \overline{\ddot{u}_{\mathrm{Tr}}}. \tag{17}$$

$\overline{I_{\mathrm{SRD2}}}$ and $\overline{i_i}$ are the averaged signal currents and $\overline{\ddot{u}_{\mathrm{Tr}}}$ the according average transformation ratio of the transformer (transistor).

In the time interval in which the stored signal charge is recalled and the output pulses are generated, (16) is valid. (SRD_1 is in the conducting and SRD_2 in the cutoff state, see Fig. 12.) The total charge gain of both phenomena delivers with $V_3 \ll V_p$

$$v_q = v_{q\mathrm{Tr}} v_{qd} = \frac{\overline{\ddot{u}_{\mathrm{Tr}}}}{1 + \overline{\ddot{u}^2_{\mathrm{Tr}}}}. \tag{18}$$

By using ideal transformers ($\ddot{u}_{\mathrm{Tr}} = \ddot{u}_{\mathrm{Tr}'} > 1$) $v_q < 1$ is always valid.

The charge gain $v_q > 1$ that is actually obtained is caused by the fact that at a bit rate of 1 Gbit/s of the signals the charging of the diodes by the input pulses lasts longer ($\simeq$650 ps) than discharging them ($\simeq$100 ps), see Fig. 10. Therefore, a considerably higher average current gain of the transistor (transformer) is achieved in the charging time of the diode than in the discharging time ($\overline{\ddot{u}_{\mathrm{Tr}}} > \overline{\ddot{u}^2_{\mathrm{Tr}'}}$).

With these considerations three conditions for obtaining a high charge gain, and consequently, an essential voltage and power gain can be given.

1) The employed diodes should be chosen in such a way that the charging times of the diodes are much higher than their discharging times at a given bit rate of the signal pulses. In general the discharging times approximately amounts to twice the voltage rise times of the diodes (optimum operating point).

2) A real transformer (transistor) must have a time dependent transformation ratio $\ddot{u}$ within the period T. The stronger $\ddot{u}$ increases with time t, the better it is. In addition to this, $\ddot{u}_{\mathrm{Tr}'} \simeq 1$ should be valid.

Using transistors employed as transformers, a calculation yields the following: $\tau_T \simeq t_r \simeq T_{p1}/2$ (τ_T: transit time of the transistor, t_r: rise time of the diodes). With $f_T = (2\pi\tau_T)^{-1}$ and $T_{p1} \simeq 80$ ps the optimum current gain–bandwidth product f_T of the chosen (ideal) transistors follows to be $f_T \simeq 4$ GHz. In real transistors f_T should be somewhat higher because parasitic elements, e.g., series inductances in the emitters and case capacitances, reduce the effective current gains.

3) The transmission ratios of the transformers are very high if the DDR is operated at low bit rates of the signal pulses. This leads to a low value of $R_s/\ddot{u}^2$ loading the pump voltages. In this case the pump voltage in the lines 3 and 4 are not high enough for switching the diodes.

In Fig. 13 the computed output-pulse amplitudes of the DDR versus f_T of the transistors are shown. The dashed curve 2 is in good agreement with the statement of point 2). This curve was obtained with the assumption that the series inductances of the emitter of the transistors as well as of the SRD's are zero. Assuming existing inductances ($L = 1.5$ nH) curve 1 is obtained. The maximum output-pulse amplitudes are reached here at higher f_T. The employed transistors had the nearly optimum current gain-bandwidth product of $f_T = 8$ GHz (NEC, V 981 S).

Fig. 14 shows the computed amplitudes of the output pulses of the DDR versus signal-pulse bit rates, under the condition of input pulses which have both constant amplitudes (44 mV) and half-widths ($T_{pi} = 100$ ps). At high bit rates (pump frequencies, f_p) the charging times for the input pulses are also very small. In this bit-rate range the storable signal charges increase approximately linearly

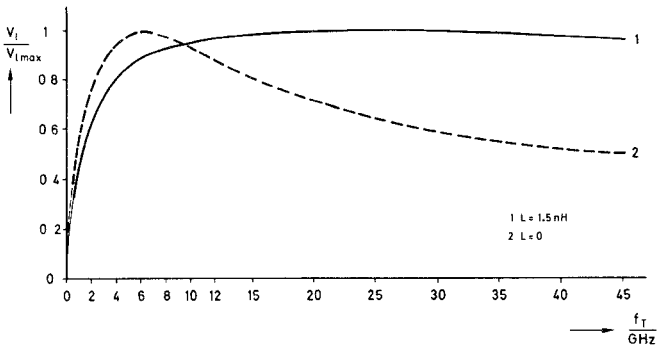

Fig. 13. Computed output-pulse amplitudes of the DDR versus the current gain-bandwidth product (f_T) of transistors.

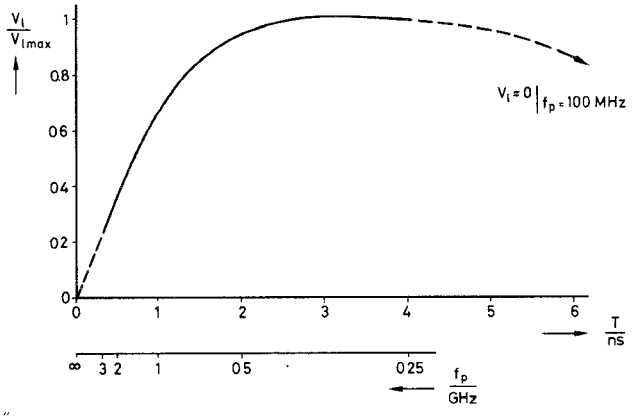

Fig. 14. Computed output-pulse amplitudes of the DDR versus the period (T) of the signal pulses. The half-width of the input pulses is held constant ($T_{pi} = 100$ ps).

with time and therefore, also the amplitudes of the output pulses. The output pulses reach a maximum amplitude if within sufficiently long charging times the whole signal charge can be stored in the SRD ($T > 2$ ns). If the bit rate of the input pulses is decreased further ($T > 4$ ns) the stated circumstances of point 3) become effective and the output-pulse amplitudes are decreased. Simultaneously their half-widths are increased. At bit rates of about 100 Mbit/s no output pulses can be regenerated with the employed transistors.

In Fig. 15 the computed insertion voltage gain of the DDR versus the bit rate (pump frequency, f_p) of the signal pulses is shown. For obtaining a realistic operation of the DDR, the half-widths T_{pi} of the input pulses were related to the period $T (T_{pi} = T/3)$. At high bit rates ($f_p > 1$ GHz) the voltage gain is approximately a square-law function of the period T. This is an extension of the linear function of the voltage gain versus the pump frequency ($f_p > 1$ GHz) shown in Fig. 14. At lower bit rates ($f_p < 1$ GHz) the insertion voltage gain presented in Fig. 15 should increase linearly with increased period T because the whole signal charges can be stored in the SRD. However, the circumstances stated in point 3) now become effective and the slope of the voltage-gain curve decreases with increased period T. At a bit rate of the input signals of 250 Mbit/s

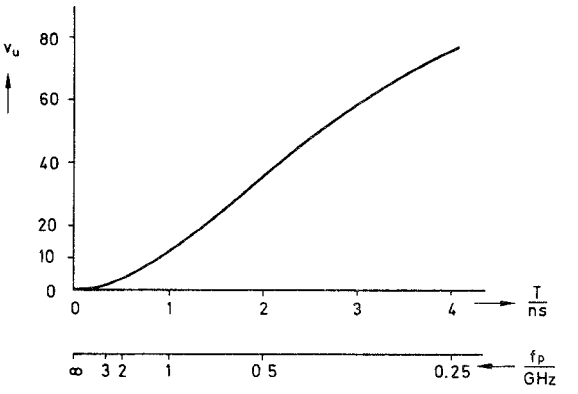

Fig. 15. Computed insertion voltage gain of the DDR versus the period (T) of the signal pulses. The half-widths of the input pulses are related to the period ($T_{pi} = T/3$).

the computed insertion voltage gain of the DDR is about $v_u = 80$. If signal pulses with bit rates much lower than 250 Mbit/s are to be regenerated, both transistors with smaller f_T (than $f_T = 8$ GHz) and SRD's having higher carrier lifetimes (than $\tau = 15$ ns) should be used.

A further essential property of the DDR can be explained by the curve of the emitter currents of the transistors shown in Fig. 10(c). In addition to the input signals—supplying the bases—the transistors are driven by the voltages V_3 and V_4 at their emitters. The transistor-current drops are caused by the resonant half-waves V_3 and V_4 which both occur during the nonconducting times of the SRD's. The transistors must not reach the cutoff state; this can be ensured by sufficiently high bias currents.

After the resonant half-waves the transistor currents rise with rise times of about 300 ps. The rise times are determined by charge storage in the diffusion capacitances of the transistors. If the currents rise unequally—caused by, e.g., unequal rise times or unequal current drops—different transistor currents exist in the times of conducting diodes. The differences in current are stored in the SRD's like signal charges. These false charges (carry charges) simulate not existing signal charges.

By using identical transistors the rise time of their currents are also equal to one another. The values of the current drops depend on the temporal switching points of the SRD's; three operating ranges have to be considered.

1) The diodes switch before the maxima of the pump voltages are reached. Then the maximum of the reverse voltage of the first switching diode is smaller than that of the later switching diode. In this way, an input pulse causes, via the reverse voltages V_3 and V_4, a reaction effect on the transistors. This creates a carry charge which is stored in the SRD's within the following bit period. If the diodes switch before the maxima of the discharging pump half-waves, the carry charge increases the stored signal charge of the next bit period and the corresponding output pulses are increased in amplitude.

2) The diodes switch a short time after the maxima of the pump voltages. In this case the currents of the transistors rise identically to one another and no carry charge is generated.

3) If the diodes switch still later, a carry charge is generated again. Now the stored signal charge of the following bit period is reduced.

The value of the carry charge depends on the position of the switching points related to the maxima of the pump voltages and is controlled by adjusting the bias voltages V_1 and V_2.

The operation of the DDR as described by the case 1) is not applicable and without any importance. Case 2) describes the operation mode suitable if the input pulses (at the emitters of the transistors) have decayed to zero at the end of the belonging bit period. This demand can be fulfilled, if short input pulses ($T_{pi}<200$ ps at a bit rate of 1 Gbit/s) and sufficiently fast switching transistors are available.

The most interesting operation of the DDR, however, is described in case 3) and is utilized if long input-pulses at the emitters of the transistors have not decayed to zero at the end of the belonging bit period. There, those parts of signal charges which are transmitted into the following bit periods can be compensated by the carry charges. In this way, input signals with half-widths as long as the period T or NRZ-format signals can be regenerated.

In Fig. 16 measured curves (1 and 1′) and computed curves (2 and 2′, 3 and 3′) describe the amount of the carry charge versus the bias voltages V_1 and V_2 of the DDR. The input signals and the operation voltages are the same as presented in Fig. 8 and Fig. 10. The carry charges are expressed by the amplitudes of the output voltages and the bias voltages are represented by $\Delta V_{1,2}= V_{1,2}-V_{1,2c}$, where V_{1c} and V_{2c} are the bias voltages producing no carry charge.

The curves 2 and 2′ were obtained by assuming inductances of $L=1.5$ nH in series to the emitters of the transistors as well as to the SRD's. For computing the curves 3 and 3′ the series inductances were set to zero.

Curves 1, 2, and 3 represent the amplitudes of first pulses arriving after some zero-bit signals, and the curves 1′, 2′, and 3′ characterize the amplitudes of the then following pulses. The first pulses show their maximum amplitudes at bias voltages of $V_{1,2}\simeq V_{1,2c}$, at which the diodes switch near the maxima of the pump voltages. If the diodes go into the cutoff states long before the pump-voltage maxima are reached ($\Delta V_{1,2}<0$), the decrease of the conducting times of the SRD's becomes effective. Then the storable signal charges also decrease leading to smaller output signals. If the switching of the SRD's occur very late in the period, that is in a region of low instantaneous pump voltage, then the output pulses are broadened and their amplitudes lowered (computed curve 3). In contrast, the output pulse amplitudes represented in the measured curve 1 keep their full amplitudes for high $\Delta V_{1,2}$ because the excited resonant half-waves V_3 and V_4 reach

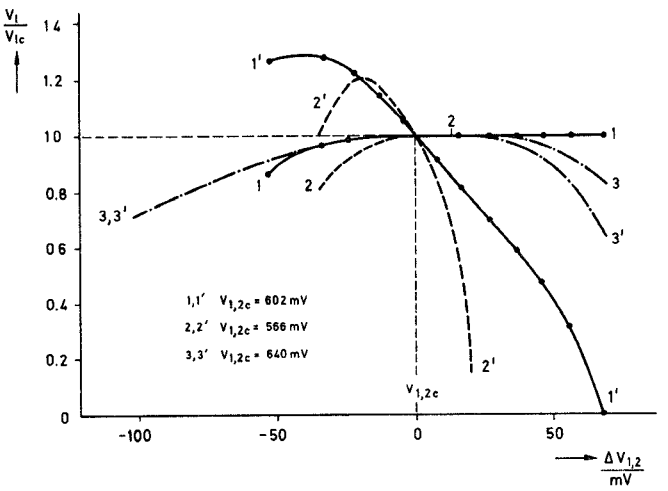

Fig. 16. Influence of the carry charge on the output-pulse amplitudes of the DDR versus the bias voltages $\Delta V_{1,2}=V_{1,2}-V_{1,2c}$. 1 and 1′ are measured curves; 2 and 2′, 3 and 3′ are computed curves.

approximately double the instantaneous value of the pump voltage (see Fig. 10(b)).

The behavior of the second output pulses is quite different from that of the first pulses. In the range of $\Delta V_{1,2}<0$ the carry charge increases the output-pulse amplitudes, whereas for $\Delta V_{1,2}>0$ it decreases them. For reaching the point of zero carry charge (compensating point) the bias voltages V_1 and V_2 must be precisely adjusted.

The series inductances of the emitters of the transistors and of the SRD's have a considerable influence on the slope of the curves 1′ and 2′, the slopes increasing with increasing inductances. In the realized DDR the series inductances are about 1 nH.

If a zero bit (no pulse) follows a one bit (pulse), carry charge pulses (false pulses) are generated in the output lines during the zero-bit period in the case of not adjusted compensating point. The amplitudes of these false pulses equal the difference of curves 1 and 1′.

Fig. 17 shows the temporal position of the output pulses (ΔT) relative to the maximum of the pump voltage versus $\Delta V_{1,2}=V_{1,2}-V_{1,2c}$. At $\Delta T>0$ the output pulses are generated later than the pump voltage maximum. In the measured curve 1 as well as in the computed 2, adjustment to the compensation point ($V_{1,2c}$) makes the diodes switch a short time after the pump voltage maximum. This circumstance is corroborated by Fig. 10(b) and 10(d).

For obtaining the optimum operation point (see Figs. 6 and 7) the amplitude of the applied pump voltage has to be adjusted depending on the signal charges of the input pulses. Therefore, it is necessary to know the influence of the pump-voltage amplitude ($V_{p3,4}$) on the temporal switching points (ΔT) of the DDR. In Fig. 18 this correlation is shown.

As can be seen, the SRD's switch later with increased pump-voltage amplitude. This effect is also caused by an interaction of transistors and SRD's. With increasing

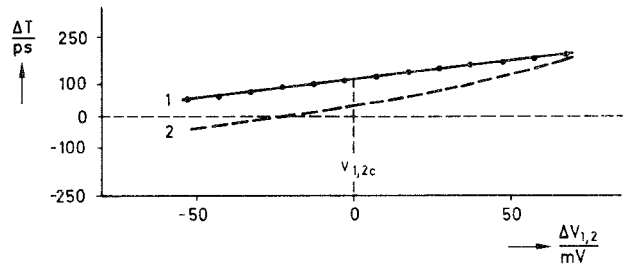

Fig. 17. Temporal position of the output pulses in relation to the maximum of the discharging pump half-wave versus the bias voltages $\Delta V_{1,2}$.

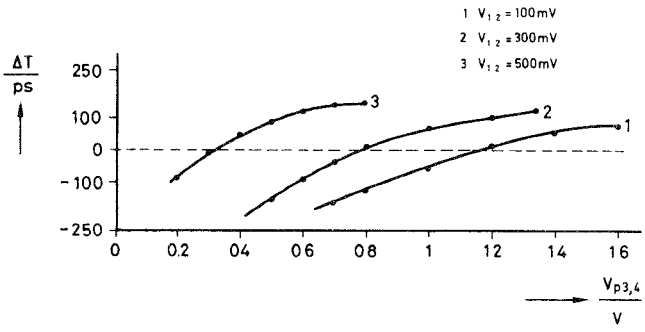

Fig. 18. Temporal position of the output pulses in relation to the maximum of the discharging pump half-wave versus the undistorted pump-voltage amplitudes ($V_{p3,4}$) on lines 3 and 4.

pump voltages $V_{p3,4}$ the reverse voltages across the SRD's increase, too, and so do the drops of the transistor currents. The latter lead to an additional charging of the SRD's causing later switching of the diodes.

For adjusting the compensating point both the pump voltages $V_{p3,4}$ and the bias voltages V_1 and V_2 must be considered. Their interrelation for reaching the compensating point is represented in Fig. 19.

Apart from the described parameters the voltage gain of the DDR depends on the short-circuit current gain (B_0) for low frequencies of the employed transistors. In Fig. 20 computed output voltages versus B_0 are shown. (Bit rate of the input signals: 1 Gbit/s, $V_i = V_{i0}/2 = 44$ mV). As can be expected, increased half-widths of the input pulses lead to increased output voltages. The existence of a maximum of the voltage gain in the range of $B_0 \simeq 35 \cdots 70$, however, is of some interest. At small values of B_0 the signal currents of the transistors increase with increased B_0 because the maximum value of B_0 can be reached within the conducting times of the SRD's. At high values of B_0 this is impossible. So the amplified signal charges as stored in the SRD's do not increase infinitely with increasing B_0 but reach a maximum. The employed transistors exhibited a short-circuit current gain for low frequencies of $B_0 = 71$.

IV. Conclusion

In the pulse regenerator circuit "DDR" an ultra broad-band hybrid tee is used for the first time in a modified version for broad-band digital applications. The DDR can regenerate signal pulses with bit rates up into the gigabit-per-second range, the shape of the input pulses having no influence on the shape of the output pulses. Only the charge of the input pulses determines the amplitude of the output pulses.

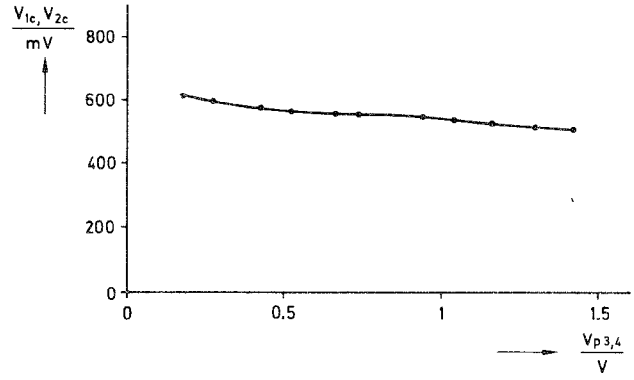

Fig. 19. Bias voltages V_{1c} and V_{2c} of the compensating point of the DDR versus the undistorted pump-voltage amplitudes ($V_{p3,4}$) on lines 3 and 4.

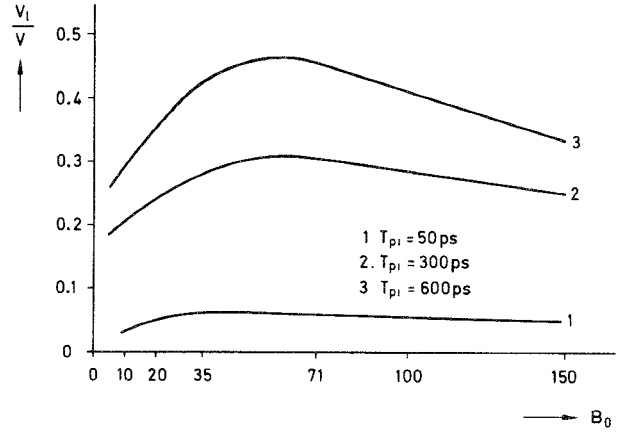

Fig. 20. Computed output voltages of the DDR versus short-circuit current gain (B_0) of the transistors. (Transistors of $f_T = 8$ GHz.)

At a rate of 1 Gbit/s of the signal pulses an insertion voltage gain of 20 dB was measured. Operating the DDR in a push–pull mode the voltage gain doubled to 26 dB. At a bit rate of 250 Mbit/s the voltage gain was computed to about 38 dB.

Although the internal interactions between the components of the DDR are complex, the circuit can be optimized without problems. An optimum operation point of the DDR exists for input pulses of any shape, the only limitation being that their widths, measured at about 10 percent of their amplitudes, must not be longer than two bit periods. The DDR is adjusted by first tuning the pump voltage to its optimum value (optimum operating point) and then setting the bias voltages V_1 and V_2 for zero carry charge (compensating point).

The ability to regenerate relative broad input pulses—compared to their period—is caused by a compensation of those parts of the signal charges stored in their following bit periods by an adjustable "carry charge". Therefore, RZ-format signals, e.g., in digital PCM-communica-

tion systems can be fully regenerated, even if they are broadened to an NRZ-format by the dispersion of the transmission lines.

Drift of the operation point and changes in symmetry between the lines caused by temperature effects, were not observed.

Because of its very short output pulses the DDR can be employed—e.g., in a simplified version without transistors—in time-division multiplexers [8], [18]–[20]. Such multiplexer circuits were realized which provide RZ-format output-pulse streams with bit rates up to 7.84 Gbit/s for PCM-type input tributaries at 1.12 Gbit/s. Output voltages of 2 V (maximum: 10 V with the employed step recovery diodes) were obtained across a load of 50 Ω. Another multiplexer experiment was performed that provided an NRZ-format output pulse stream of 16 Gbit/s bit rate and also 2-V output voltage across a load of 50 Ω [20].

Acknowledgment

The author wishes to thank Prof. B. G. Bosch for guidance and J. Kirchhoff for helpful assistance in the computation regarding the diode differential regenerator.

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